REMARKS

Claims 43, 45, 47 and 49 are amended, no claims are canceled or added; as a result, claims 26-49 remain pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statement filed on May 22, 2000, marked as being considered and initialed by the Examiner, be returned with the next official communication. A copy of the Information Disclosure Statement, 1449 Form, listed documents and USPTO date stamped postcard are enclosed for the examiner's convenience.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection, for example, rejections under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§102 Rejection of the Claims

Claims 26, 29, 32, 35-39, and 40 were rejected under 35 USC § 102(e) as being anticipated by Langendorf et al. (U.S. Patent No. 6,505,282). Applicant respectfully traverses.

Claim 26 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of *burst* extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the *burst* extended data out mode (emphasis added)." Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out mode or a set of access control signal timing requirements as recited in claim 26. Hence, Langendorf does not teach each of the elements of claim 26. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 26. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 26.

Claim 29 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of *burst* extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the *burst* extended data out mode (emphasis added)." Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out mode or a set of access control signal timing requirements as recited in claim 29. Hence, Langendorf does not teach each of the elements of claim 29. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 29. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 29.

Claim 32 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of *burst* extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the *burst* extended data out mode . . . a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide the *first set of access control signals* to the memory *at a first time* and the *second set of access control signals* to the memory *at a second time* (emphasis added)." Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out mode or a set of access control signal timing requirements as recited in claim 32. For example, applicant can not find where Langendorf discloses providing the first set of access control signals at a first time and the second set of access control signals at a second time as recited in claim 32. Hence, Langendorf does not teach each of the elements of claim 32. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 32. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 32.

Claim 35 recites, in part, "a *first bank* of *burst* extended data out memory coupled to the memory controller to receive a plurality of access control signals; and a *second bank* comprised of a memory type selected from the group consisting of *extended data out memory* and *fast page mode* memory . . . wherein the memory controller drives the access control signals in a *first mode* to provide access to the *first bank*, still further wherein the memory controller drives the access control signals in a *second mode* to provide access to *the second bank* (emphasis added)."

Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a first bank of burst extended data out memory and a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory as recited in claim 35. For example, applicant can not find where Langendorf discloses access control signals in a first mode and a second mode as recited in claim 35. Hence, Langendorf does not teach each of the elements of claim 35. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 35. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 35.

Claim 36 depends from claim 35 and is believed to be allowable for at least the same reasons as stated above with regard to claim 35.

Claim 37 recites, in part, "wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of *burst* extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a *first set* of requirements for the *burst* extended data out memory and a second set of requirements for the second type of memory (emphasis added)." Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out memory as recited in claim 37. Hence, Langendorf does not teach each of the elements of claim 37. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 37. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 37.

Claim 38 recites, in part, "a first bank of *burst* extended data out memory (emphasis added)." Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out memory as recited in claim 38. Hence, Langendorf does not teach each of the elements of claim 38. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 38. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 38.

Claim 39 recites, in part, "a memory type selected from the group consisting of *burst* extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the *burst* extended data out memory . . . (emphasis added)." Applicant can not find these

features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out memory as recited in claim 39. Hence, Langendorf does not teach each of the elements of claim 39. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 39. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 39.

Claim 40 recites, in part, "a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of *burst* extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the *burst* extended data out mode . . . (emphasis added)." Applicant can not find these features in Langendorf. For example, applicant can not find where Langendorf discloses a burst extended data out mode or a first set of access control signals as recited in claim 40. Hence, Langendorf does not teach each of the elements of claim 40. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 40. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 40.

Claims 26, 29, 32, 35-39, and 40 were rejected under 35 USC § 102(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp. 1-67, 11/96 (INTEL). Applicant respectfully traverses.

The Office Action states that as to claims 26, 29, 32 and 35-39, EN discloses the invention as claimed. The Office Action then relies on inherency and cites INTEL to support the theory of inherency.

EN specifically does not disclose "a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode" as claimed by the Appellant in claim 26, or "a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode" as claimed in claim 29. EN also does not disclose "a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode" as claimed in claims 32 and 40, "a first bank of burst extended data out memory" as claimed in claims 35, 36, and 38, or "a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group

consisting of burst extended data out memory and a second type of memory" as claimed in claims 37 and 39.

The Office Action rejects claims 26, 29, 32, 35-40 under 35 USC § 102(a). However, EN does not meet the statutory requirements of 35 USC § 102(a). EN merely discloses "Intel, by the way, is now readying its "Triton" PCI chipset, which it was demonstrating privately during Fall Comdex." However, EN does not provide evidence that the present invention as defined by the pending claims was known or used by others in this country. Moreover, there is no public disclosure as EN explicitly states that Intel is *readying* its Triton chip set after *privately* demonstrating the chip set at Fall Comdex. There is no disclosure of any feature in the Triton chip set. Still further, EN does not describe the invention in a printed publication before the invention by the applicant. Reconsideration and withdrawal of the 35 USC § 102(a) rejection are requested.

Intel also does not disclose these elements since operations using burst EDO memories are not discussed. As noted above, Intel merely teaches the use of standard page mode and EDO RAM in main memory. See Intel, Pg. 41, Col. 2, para. 4. While it is asserted in the Office Action that FIG. 1 and pgs. 1, 24, 31, and 41-45 of Intel disclose burst operation, the Appellants' representative was only able to find references to synchronous burst and pipelined burst SRAMS, and not burst EDO memories. (Pg. 34, Col. 2, para. 3).

The use of devices operable in burst EDO and another mode (claims 26, 29, 32, and 40), or using burst EDO memory in one bank and a different type of memory in a second bank (claims 35-39) are not disclosed in this reference. Thus, the assertion that "These inherent features are disclosed by Intel ..." is incorrect.

Claimed features are not inherent in EN

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be

established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

EN on its face undermines the basis for the use of inherency to read features in EN that are not specifically found therein. EN states that "Intel, by the way, is now readying its "**Triton**" PCI chipset, which it was demonstrating privately during Fall Comdex." Applicant submits that "readying" means that the Triton PCI chipset was not complete and may or may not have included the features found in INTEL as INTEL is date November 1996. Moreover, "demonstrating privately" means that the Triton PCI chipset was not disclosed to the public and thus not prior art as of Fall Comdex or the date of EN.

Reliance on MPEP 2124 and 2131.01 is incorrect

Generally, a non-patent document is prior art and can be used in rejecting claims under 35 U.S.C. §103 if its publication date precedes the filing date of the application.

The present application is a continuation of an application that was filed on June 1, 1995, which claims CIP status to an application filed December 23, 1994. The Intel document has a publication date of November 1996. Clearly, well over a year -at least about 15 months- after the effective filing date of the present application. Accordingly, INTEL is not available as a prior art document under the basic rule for available prior art for use in 35 U.S.C. §103 rejections.

In order for the examiner to use INTEL it must fall under one of the narrow exceptions to the rule that a non-patent document must predate the filing date of the application. Some narrow instances where a document need not antedate the filing date are set forth in MPEP §2124. The examiner cites MPEP §2124 for supporting his use of INTEL as prior art in rejecting the claims under 35 U.S.C. §102(a). MPEP 2124 provides exception to the rule that the critical reference date must precede the filing date of an application. MPEP 2124 states

> In certain circumstances, references cited to show a universal fact need not be available as prior art before applicant's filing date. In

> re Wilson, 311 F.2d 266, 135 USPQ 442 (CCPA 1962). Such facts include the characteristics and properties of a material or a scientific truism. Some specific examples in which later publications showing factual evidence can be cited include situations where the facts shown in the reference are evidence "that, as of an application's filing date, undue experimentation would have been required, In re Corneil, 347 F.2d 563, 568, 145 USPQ 702, 705 (CCPA 1965), or that a parameter absent from the claims was or was not critical, In re Rainer, 305 F.2d 505, 507 n.3, 134 USPQ 343, 345 n.3 (CCPA 1962), or that a statement in the specification was inaccurate, In re Marzocchi, 439 F.2d 220, 223 n.4, 169 USPQ 367, 370 n.4 (CCPA 1971), or that the invention was inoperative or lacked utility, In re Langer, 503 F.2d 1380, 1391, 183 USPQ 288, 297 (CCPA 1974), or that a claim was indefinite, In re Glass, 492 F.2d 1228,1232 n.6, 181 USPQ 31, 34 n.6 (CCPA 1974), or that characteristics of prior art products were known, In re Wilson, 311 F.2d 266, 135 USPQ 442 (CCPA 1962)." In re Koller, 613 F.2d 819, 823 n.5, 204 USPQ 702, 706 n.5 (CCPA 1980) (quoting In re Hogan, 559 F.2d 595, 605 n.17, 194 USPQ 527, 537 n.17 (CCPA 1977) (emphasis in original)). However, it is impermissible to use a later factual reference to determine whether the application is enabled or described as required under 35 U.S.C. 112, first paragraph. In re Koller, 613 F.2d 819, 823 n. 5, 204 USPQ 702, 706 n.5 (CCPA 1980). References which do not qualify as prior art because they postdate the claimed invention may be relied upon to show the level of ordinary skill in the art at or around the time the invention was made. Ex parte Erlich, 22 USPQ 1463 (Bd. Pat. App. & Inter. 1992).

Applicant requests that the examiner indicate the specific basis for reliance on this MPEP section to clarify issues for appeal. Applicant submits that Intel does not prove the characteristics and properties of a material or a scientific truism.

Based on the undersigned's reading of MPEP 2124, the examiner appears to be relying on In re Wilson. Applicant respectfully submits that such reliance is misplaced. Wilson allows the use of publications that have a date after the filing date of the application to prove a universal fact. The court in Wilson first found the claims at issue to be obvious in view of acknowledged prior art and a prior art reference. The admitted prior art and the prior art reference both predated the application filing date. Thus, two pieces of prior art as defined by the statute were applied in a §103 rejection. The court did not use the publication that is subsequent to the application filing date to prove a case of *prima facie* anticipation under §102(a).

The appellant-applicant in Wilson further asserted a factual advantageous feature that resulted from the claimed inventive chemical process. The court then used the publication to create a factual suspicion on the appellant-applicant's assertion of a factual advantageous feature from the claimed chemical process.[1]

Based on Wilson, the examiner's reliance on EN to read Intel as prior art is misplaced. First, a *prima facie* case of obviousness has not been established based on prior art that one of ordinary skill had at the time of the present invention. That is, the examiner can not rely on Intel in a rejection under §102(a). Second, applicant has not submitted factual evidence under the Graham factual inquires to rebut a *prima facie* case of obviousness, which would allow the examiner to use publications that are after the present filing date to evaluate the facts set forth by the applicant.

Accordingly, applicant respectfully requests that the §102(a) rejection of the pending claims based in part on EN and Intel be withdrawn.

§103 Rejection of the Claims

Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being anticipated by Langendorf et al. in view of Christeson (U.S. Patent No. 5,822,581). Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp. 1-67, 11/96 (INTEL) and in further view of Christeson.

Applicant assumes that this rejection is an obviousness rejection under 35 USC 103(a) and not an "anticipated" as stated in the Office Action. If this assumption is incorrect, please notify the undersigned in the next paper to clarify issues for appeal.

Applicant submits that EN and Intel doe not teach all of the features of the pending claims for the reasons stated above and Intel is not prior art against the present application.

Applicant respectfully requests reconsideration of the application of Christeson as a reference against claims 27-28, 30-31, 33, 34, and 41-49. Christeson has a filing date of 29 September 1995. The effective filing date of the present application is the filing date of its

[1] In re Wilson, 1962 CCPA Lexis 170, 15-16.

parent applications, specifically, U.S. Serial No. 08/457,650 filed June 1, 1995; which is a continuation-in-part of U.S. Serial No. 08/386,894 filed February 10, 1995, now U.S. Patent No. 5,610,864; which is a continuation-in-part of U.S. Serial No. 08/370,761 filed December 23, 1994, now U.S. Patent No. 5,526,320. As each of these filing dates precedes the filing date of Christeson, applicant respectfully submits that Christeson is not a reference against the present application.

Claims 26, 29, 32, and 35-39 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al. (U.S. Patent No. 5,307,320) in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron Technical Note, pp. 5-33 thru 5-40, 4/94 and further in view of Wyland (U.S. Patent No. 5,261,064). Applicant traverses.

Applicant requests clarification of this rejection. The Office Action indicates that the rejection is under 35 USC § 103(a) but uses the term "anticipated". Applicant assumes that this is an obviousness rejection. If this assumption is incorrect, please notify the undersigned in the next action.

Claim 26 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of *burst* extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the *burst* extended data out mode (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland disclose a burst extended data out mode or a set of access control signal timing requirements as recited in claim 26. Hence, Farrer, Micron or Wyland do not teach each of the elements of claim 26. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 26. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 26.

Claim 29 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of *burst* extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the *burst* extended data out mode (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland disclose a burst extended data out mode or a set of access control signal

timing requirements as recited in claim 29. Hence, Farrer, Micron or Wyland do not teach each of the elements of claim 29. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 29. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 29.

Claim 32 recites, in part, "a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of *burst* extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the *burst* extended data out mode . . . a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide the *first set of access control signals* to the memory *at a first time* and the *second set of access control signals* to the memory *at a second time* (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland disclose a burst extended data out mode or a set of access control signal timing requirements as recited in claim 32. For example, applicant can not find where Farrer, Micron or Wyland disclose providing the first set of access control signals at a first time and the second set of access control signals at a second time as recited in claim 32. Hence, Farrer, Micron or Wyland do not teach each of the elements of claim 32. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 32. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 32.

Claim 35 recites, in part, "a *first bank* of *burst* extended data out memory coupled to the memory controller to receive a plurality of access control signals; and a *second bank* comprised of a memory type selected from the group consisting of *extended data out memory* and *fast page mode* memory . . . wherein the memory controller drives the access control signals in a *first mode* to provide access to the *first bank*, still further wherein the memory controller drives the access control signals in a *second mode* to provide access to *the second bank* (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland disclose a first bank of burst extended data out memory and a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory as recited in claim 35. For example, applicant can not find where Farrer, Micron or Wyland disclose access control signals in a first mode and a

second mode as recited in claim 35. Hence, Farrer, Micron or Wyland do not teach each of the elements of claim 35. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 35. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 35.

Claim 36 depends from claim 35 and is believed to be allowable for at least the same reasons as stated above with regard to claim 35.

Claim 37 recites, in part, "wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of *burst* extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a *first set* of requirements for the *burst* extended data out memory and a second set of requirements for the second type of memory (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland disclose a burst extended data out memory as recited in claim 37. Hence, Farrer, Micron or Wyland do not teach each of the elements of claim 37. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 37. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 37.

Claim 38 recites, in part, "a first bank of *burst* extended data out memory (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland disclose a burst extended data out memory as recited in claim 38. Hence, Farrer, Micron or Wyland do not teach each of the elements of claim 38. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 38. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 38.

Claim 39 recites, in part, "a memory type selected from the group consisting of *burst* extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the *burst* extended data out memory . . . (emphasis added)." Applicant can not find these features in Farrer, Micron or Wyland. For example, applicant can not find where Farrer, Micron or Wyland discloses a burst extended data out memory as recited in claim 39. Hence, Farrer,

Micron or Wyland does not teach each of the elements of claim 39. Thus, the office action fails to state a *prima facie* case of obviousness with respect to claim 39. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 39.

Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al., Micron, "Reduce DRAM cycle times with extended data-out", Micron Technical Note, pp. 5-33 thru 5-40, 4/94 and Wyland and further in view of Christeson. Applicant requests clarification of this rejection. The Office Action indicates that the rejection is under 35 USC § 103(a) but uses the term "anticipated". Applicant assumes that this is an obviousness rejection. If this assumption is incorrect, please notify the undersigned in the next action. Applicant again asserts that Christeson is not a reference against the pending claims. Reconsideration and allowance of claims 27-28, 30-31, 33, 34, and 41-49 are requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612)349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

BRETT L. WILLIAMS

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
612-349-9587

Date 21 July '03

By _____
Timothy B Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 21st day of July, 2003.

Amy Moriarty
Name

_____
Signature